

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Green Device Available

Applications

- Power management in half bridge and inverters
- DC-DC Converter
- Load Switch

General Description

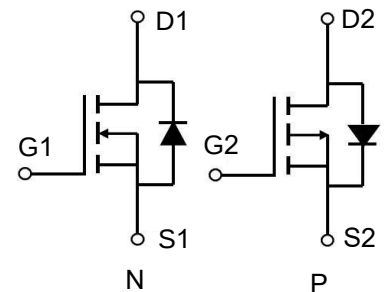
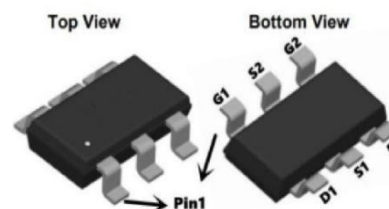
The UD8G02L is the highest performance trench N-ch and P-ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(on)}$ and gate charge for most of the synchronous buck converter applications.

The UD8G02L meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

Product Summary

BVDSS	$R_{DS(on)}$	ID
20V	14mΩ	8A
-20V	20mΩ	-8A

SOT 23-6L Pin Configurations



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-Channel	P-Channel	
V_{DS}	Drain-Source Voltage	20	-20	V
V_{GS}	Gate-Source Voltage	± 12	± 12	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	8	-8	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	5.0	-4.8	A
I_{DM}	Pulsed Drain Current ²	32	-18.8	A
EAS	Single Pulse Avalanche Energy ³	---	---	mJ
I_{AS}	Avalanche Current	---	---	A
$P_D@T_C=25^\circ C$	Total Power Dissipation ⁴	2	1.9	W
T_{STG}	Storage Temperature Range	-55 to 150	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	-55 to 150	$^\circ C$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	120	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	80	$^\circ C/W$

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	20	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=4.5V, I_D=3A$	---	14	16	$m\Omega$
		$V_{GS}=2.5V, I_D=2A$	---	17	19	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	0.5	0.75	1.2	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=16V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=16V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 12V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5V, I_D=3A$	---	---	---	S
Q_g	Total Gate Charge (4.5V)	$V_{DS}=10V, V_{GS}=4.5V, I_D=4A$	---	15	---	nC
Q_{gs}	Gate-Source Charge		---	2	---	
Q_{gd}	Gate-Drain Charge		---	5.2	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=10V, V_{GS}=4.5V, R_G=3.3\Omega, I_D=3A$	---	9	---	ns
T_r	Rise Time		---	25	---	
$T_{d(off)}$	Turn-Off Delay Time		---	37	---	
T_f	Fall Time		---	14	---	
C_{iss}	Input Capacitance	$V_{DS}=10V, V_{GS}=0V, f=1\text{MHz}$	---	700	---	pF
C_{oss}	Output Capacitance		---	132	---	
C_{rss}	Reverse Transfer Capacitance		---	114	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,4}	$V_G=V_D=0V$, Force Current	---	---	8.0	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The power dissipation is limited by 150°C junction temperature
- 4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=-250\mu A$	-20	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=-4.5V$, $I_D=-4.1A$	---	20	26	$m\Omega$
		$V_{GS}=-2.5V$, $I_D=-3A$	---	24	31	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=-250\mu A$	-0.4	-0.7	-1	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=-20V$, $V_{GS}=0V$, $T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=-20V$, $V_{GS}=0V$, $T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 12V$, $V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5V$, $I_D=3A$	---	---	---	S
Q_g	Total Gate Charge (4.5V)	$V_{DS}=-10V$, $V_{GS}=-4.5V$, $I_D=-4A$	---	19	---	nC
Q_{gs}	Gate-Source Charge		---	4	---	
Q_{gd}	Gate-Drain Charge		---	5	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-10V$, $V_{GS}=-4.5V$, $R_G=1\Omega$ $I_D=-3.3A$	---	11	---	ns
T_r	Rise Time		---	36	---	
$T_{d(off)}$	Turn-Off Delay Time		---	29	---	
T_f	Fall Time		---	8	---	
C_{iss}	Input Capacitance	$V_{DS}=-10V$, $V_{GS}=0V$, $f=1\text{MHz}$	---	1300	---	pF
C_{oss}	Output Capacitance		---	302	---	
C_{rss}	Reverse Transfer Capacitance		---	279	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,4}	$V_G=V_D=0V$, Force Current	---	---	-8	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V$, $I_S=-4.1A$, $T_J=25^\circ\text{C}$	---	---	-1.2	V

Note :

1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$

3.The power dissipation is limited by 150°C junction temperature

4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

N-Channel Typical Characteristics

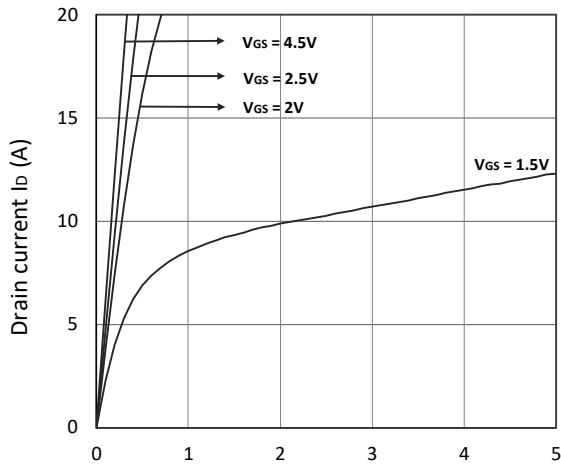


Figure 1. Output Characteristics

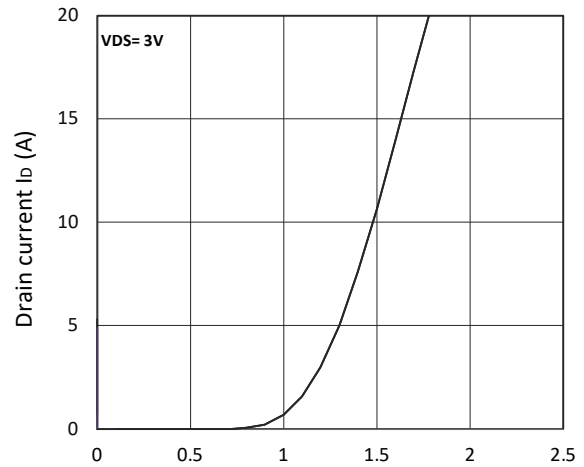


Figure 2. Transfer Characteristics

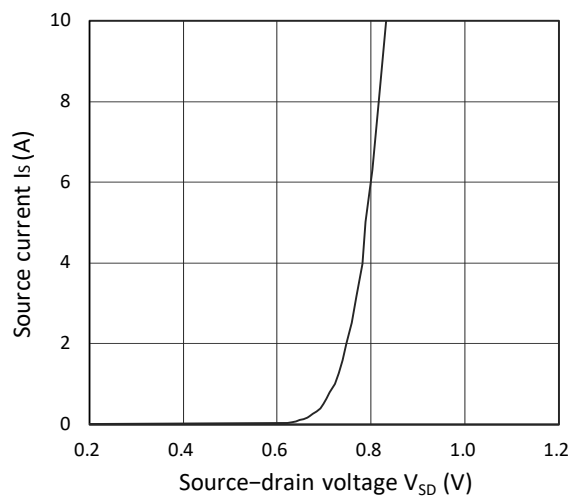


Figure 3. Forward Characteristics of Reverse

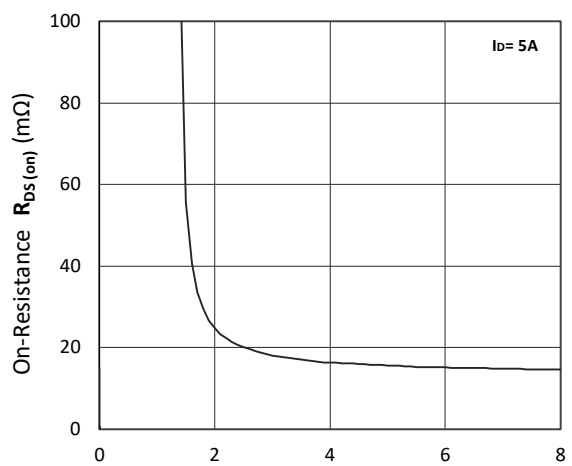


Figure 4. $R_{DS(on)}$ vs. V_{GS}

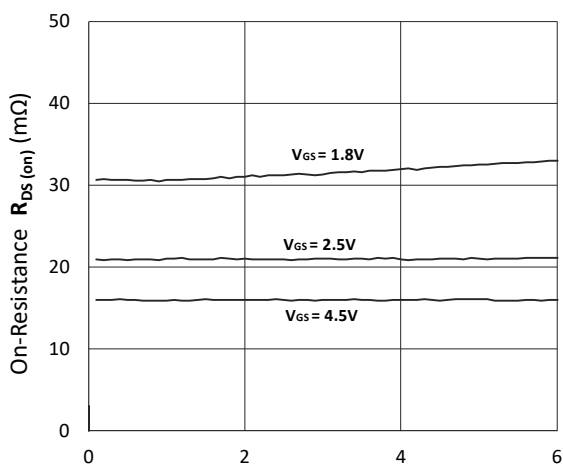


Figure 5. $R_{DS(on)}$ vs. I_D

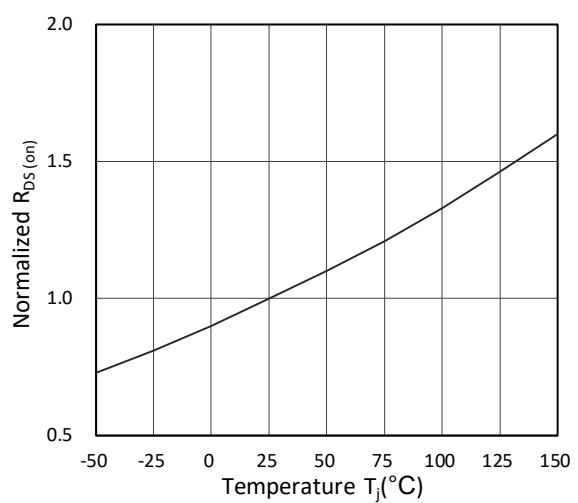


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

N-Channel Typical Characteristics

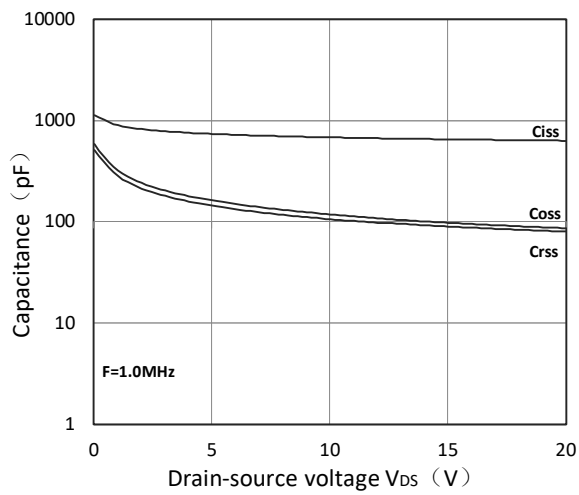


Figure 7. Capacitance Characteristics

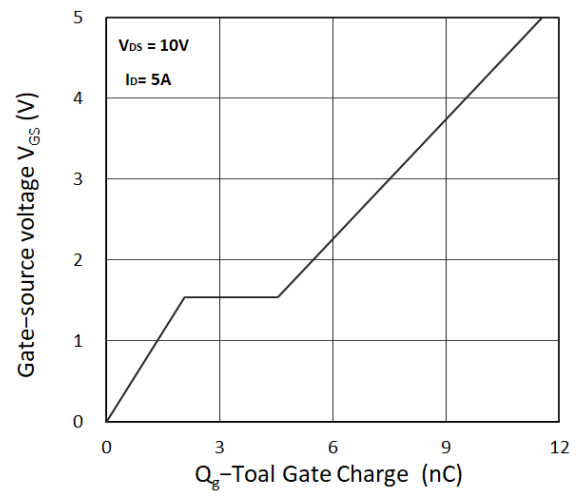


Figure 8. Gate Charge Characteristics

P-Channel Typical Characteristics

Figure 1: Output Characteristics

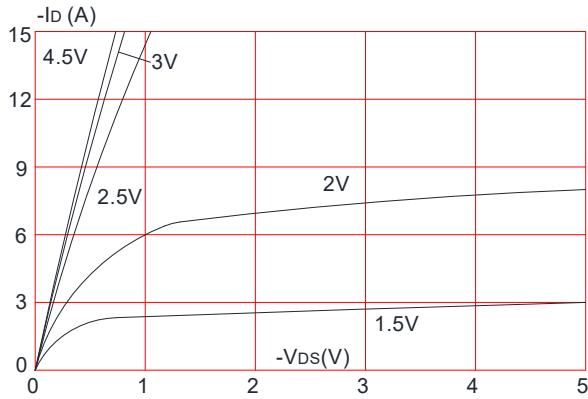


Figure 2: Typical Transfer Characteristics

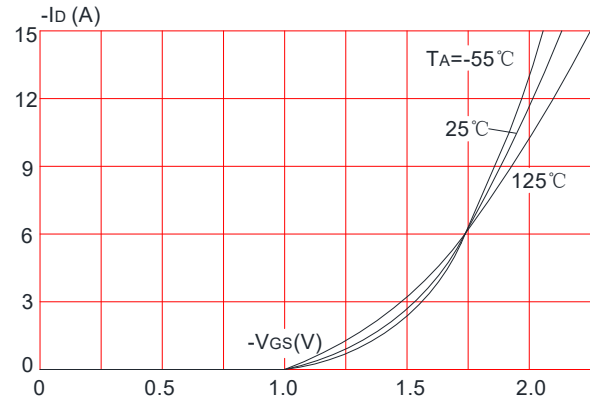


Figure 3: On-resistance vs. Drain Current

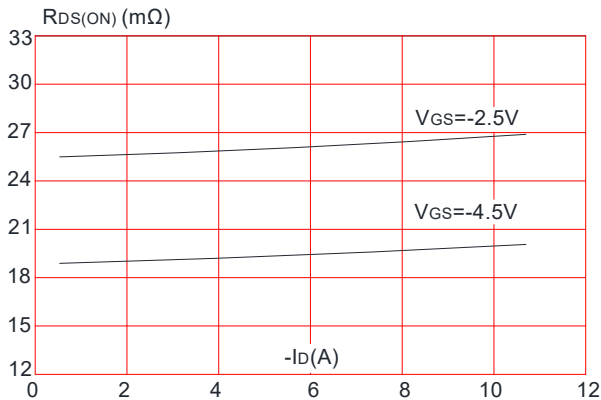


Figure 4: Body Diode Characteristics

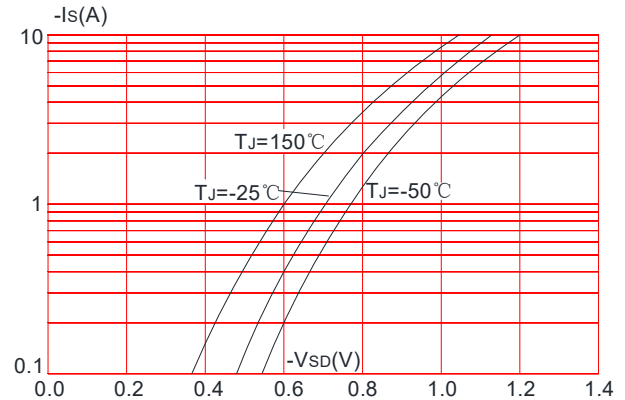


Figure 5: Gate Charge Characteristics

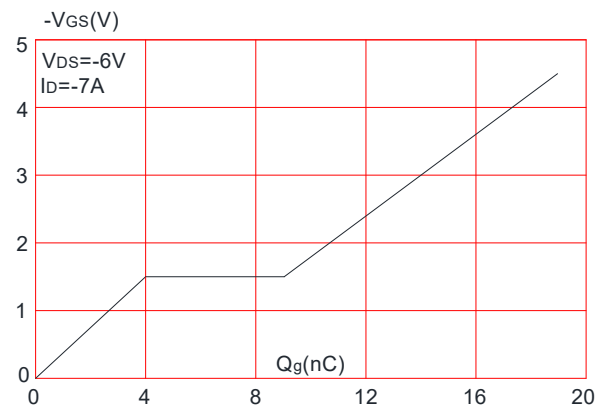
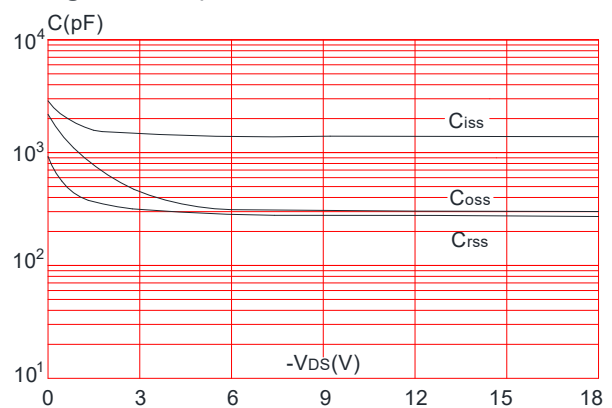


Figure 6: Capacitance Characteristics



P+N-Ch 20V Fast Switching MOSFETs

Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

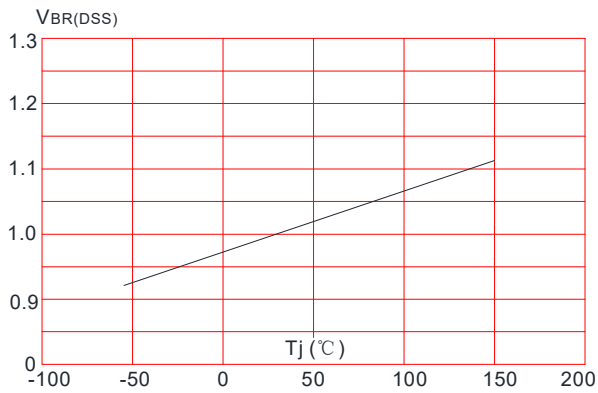


Figure 8: Normalized on Resistance vs. Junction Temperature

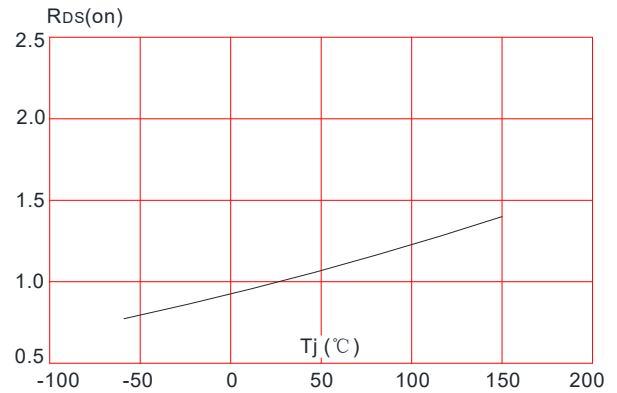


Figure 9: Maximum Safe Operating Area

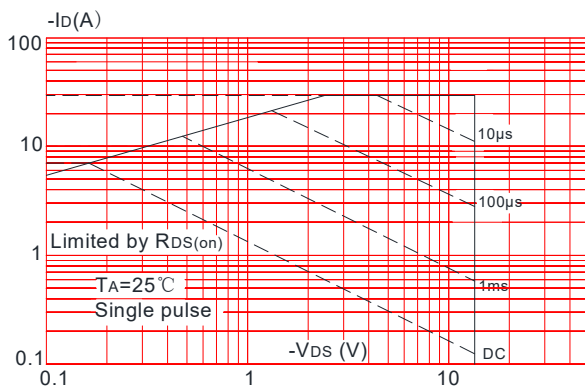


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

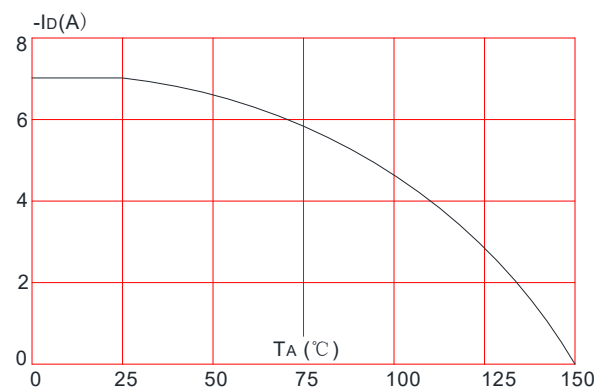
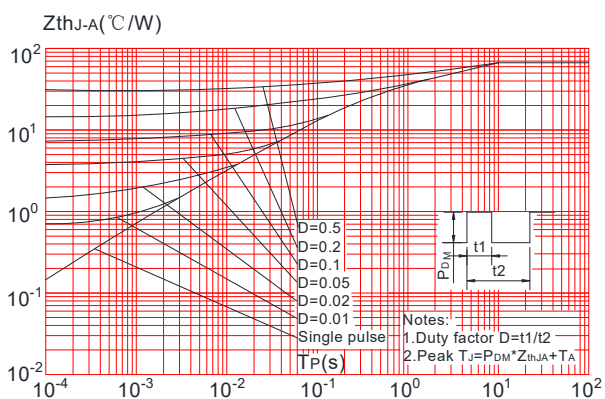
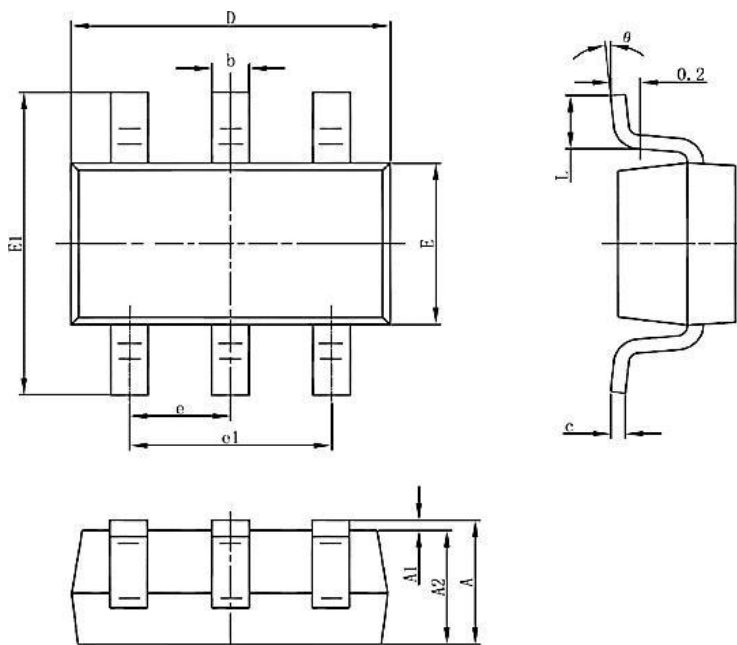


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



Package Mechanical Data-SOT23-6-Double



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
C	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 (BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0	8	0	8