

N-Ch and P-Ch Fast Switching MOSFETs

Product Summary



- ★ Super Low Gate Charge
- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

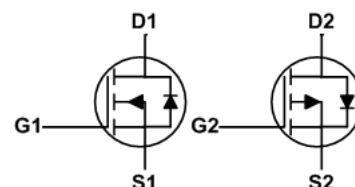
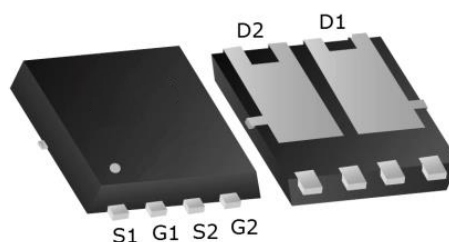
BVDSS	RDSON	ID
150V	240mΩ	6A
-150V	650mΩ	-4.1A

PDFN5060-8L Pin Configuration

Description

The UD4G15F is the highest performance complementary N-ch and P-ch MOSFETs with extreme high cell density, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The UD4G15F meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-Channel	P-Channel	
V_{DS}	Drain-Source Voltage	150V	-150V	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_D@T_A=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	6	-4.1	A
$I_D@T_A=100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	3.2	-2.7	A
I_{DM}	Pulsed Drain Current ²	21	-16	A
EAS	Single Pulse Avalanche Energy ³	9.8	12.5	mJ
I_{AS}	Avalanche Current	—	—	A
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation ⁴	40.3	7.8	W
T_{STG}	Storage Temperature Range	-55 to 150	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	62	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	3.1	$^\circ\text{C/W}$

Electrical Characteristics ($T_J = 25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	150	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=4A$	---	240	300	m Ω
		$V_{GS}=6V, I_D=0.5A$	---	---	---	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.2	2	2.5	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=150V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=150V, V_{GS}=0V, T_J=100^\circ\text{C}$	---	---	100	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	2	---	Ω
Q_g	Total Gate Charge	$V_{DS}=75V, V_{GS}=10V, I_D=4A$	---	14	---	nC
Q_{gs}	Gate-Source Charge		---	1.6	---	
Q_{gd}	Gate-Drain Charge		---	4	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=75V, V_{GS}=10V, R_G=3\Omega, I_D=4A$	---	5.8	---	ns
T_r	Rise Time		---	2.2	---	
$T_{d(off)}$	Turn-Off Delay Time		---	16.9	---	
T_f	Fall Time		---	2.6	---	
C_{iss}	Input Capacitance	$V_{DS}=75V, V_{GS}=0V, f=1\text{MHz}$	---	465	---	pF
C_{oss}	Output Capacitance		---	23	---	
C_{rss}	Reverse Transfer Capacitance		---	14	---	

Notes:

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^\circ\text{C}$.
2. The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
3. The EAS data shows Max. rating. The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=8A$
4. The power dissipation is limited by 150°C junction temperature
5. The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

P-Channel Electrical Characteristics ($T_J=25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-150	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=-10V, I_D=-1A$	---	650	780	m Ω
		$V_{GS}=-6V, I_D=-0.5A$	---	700	980	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-2	-3	-4	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=-120V, V_{GS}=0V, T_J=25^{\circ}\text{C}$	---	---	1	μA
		$V_{DS}=-120V, V_{GS}=0V, T_J=85^{\circ}\text{C}$	---	---	30	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	5	12	20	Ω
Q_g	Total Gate Charge (-10V)	$V_{DS}=-75V, V_{GS}=-10V, I_D=-1A$	6.5	10.8	15.2	nC
Q_{gs}	Gate-Source Charge		1.6	3.1	4.7	
Q_{gd}	Gate-Drain Charge		1.1	2.2	3.3	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-30V, V_{GS}=-10V, R_G=6\Omega, I_D=-1A$	---	21	32	ns
T_r	Rise Time		---	16	24	
$T_{d(off)}$	Turn-Off Delay Time		---	40	60	
T_f	Fall Time		---	18	27	
C_{iss}	Input Capacitance	$V_{DS}=-75V, V_{GS}=0V, f=1\text{MHz}$	424	706	988	pF
C_{oss}	Output Capacitance		12	23	35	
C_{rss}	Reverse Transfer Capacitance		7	13	20	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V$, Force Current	---	---	-2.2	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=-1A, T_J=25^{\circ}\text{C}$	---	---	-1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=-25V, V_{GS}=-10V, L=0.5mH, I_{AS}=-14A$
- 4.The power dissipation is limited by 150 $^{\circ}\text{C}$ junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

N-Channel Typical Characteristics

Typical Characteristics

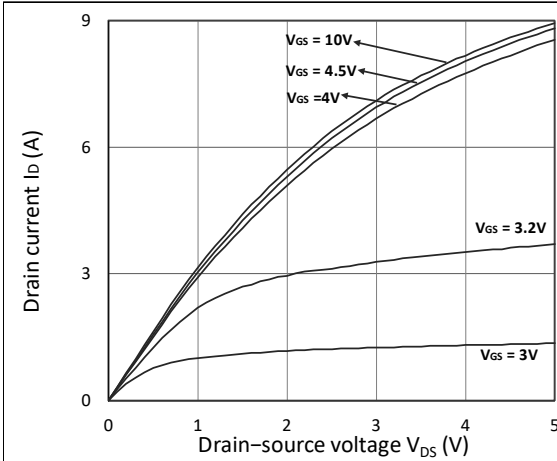


Figure 1. Output Characteristics

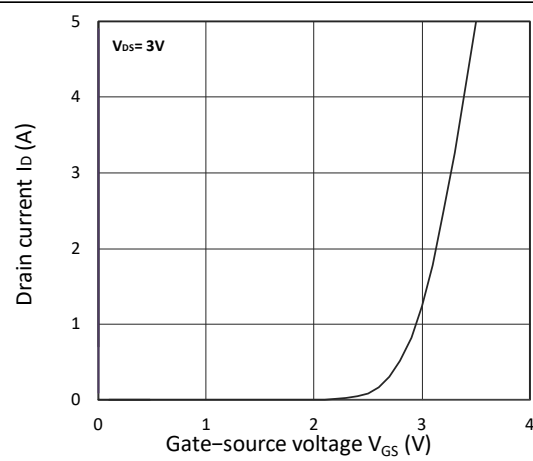


Figure 2. Transfer Characteristics

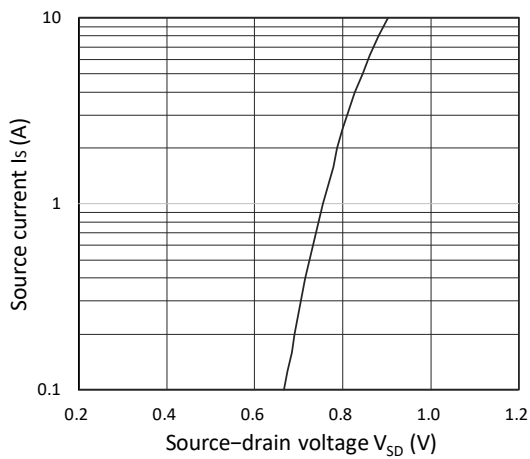


Figure 3. Forward Characteristics of Reverse

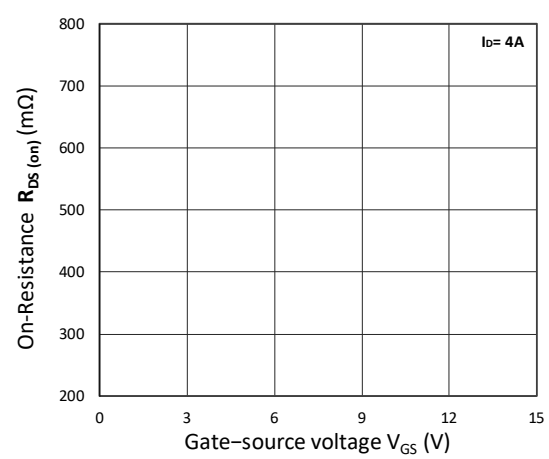


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

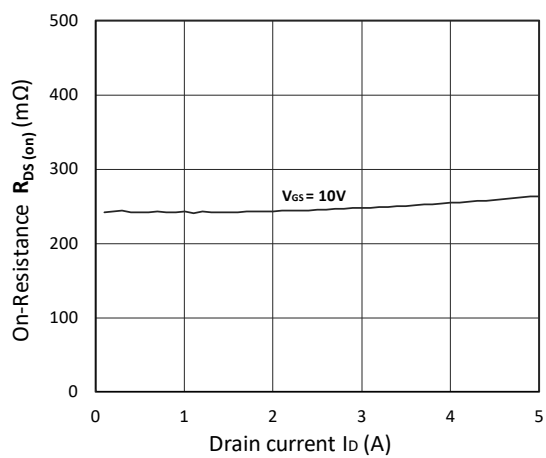


Figure 5. $R_{DS(ON)}$ vs. I_D

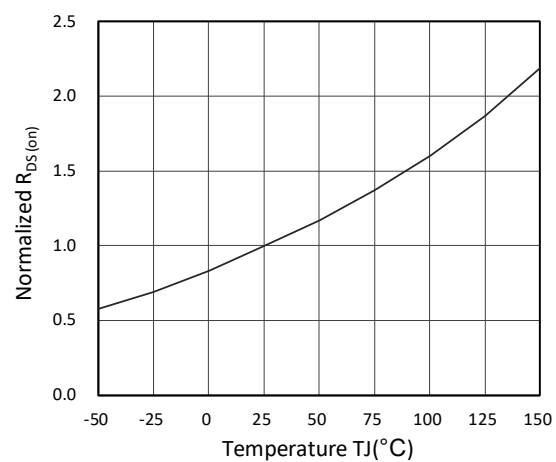


Figure 6. Normalized $R_{DS(ON)}$ vs. Temperature



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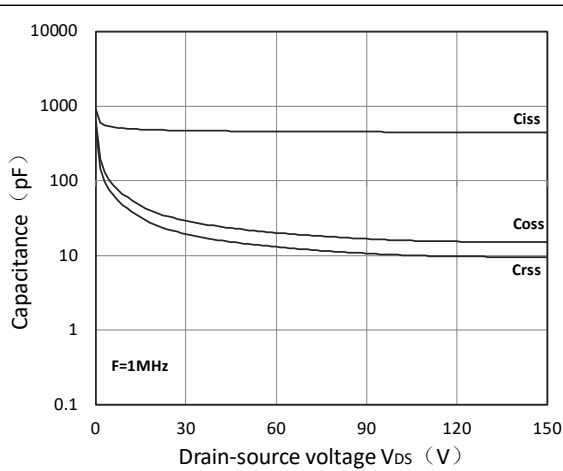


Figure 7. Capacitance Characteristics

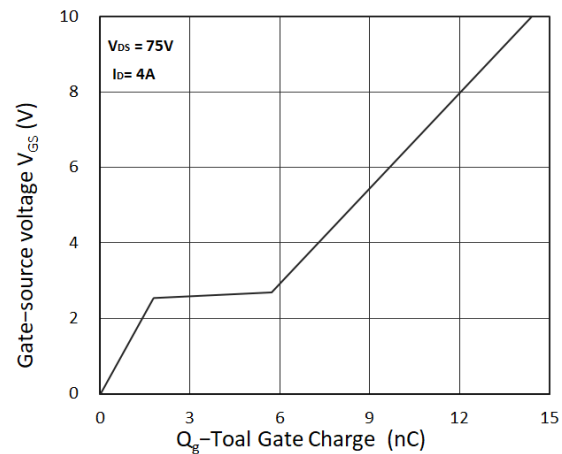


Figure 8. Gate Charge Characteristics

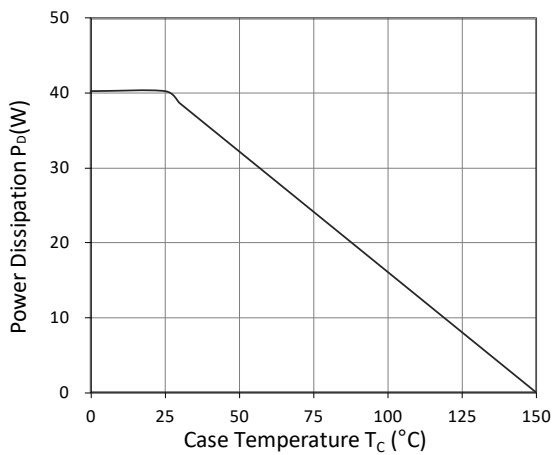


Figure 9. Power Dissipation

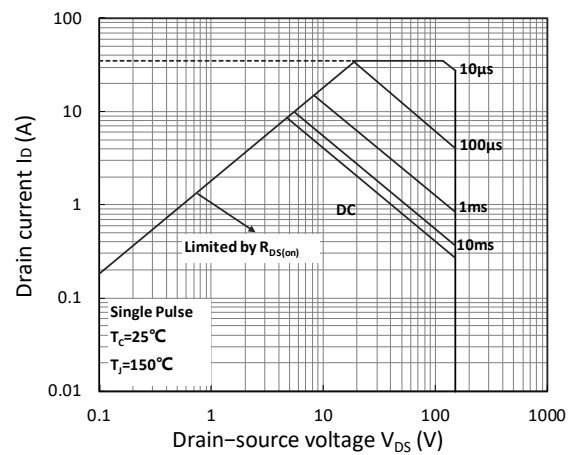


Figure 10. Safe Operating Area

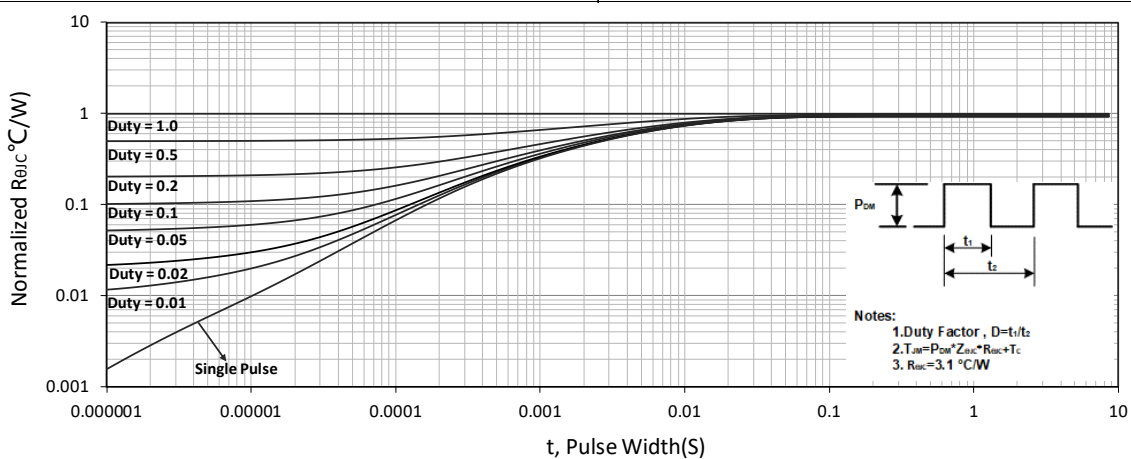


Figure 11. Normalized Maximum Transient Thermal Impedance

P-Channel Typical Characteristics

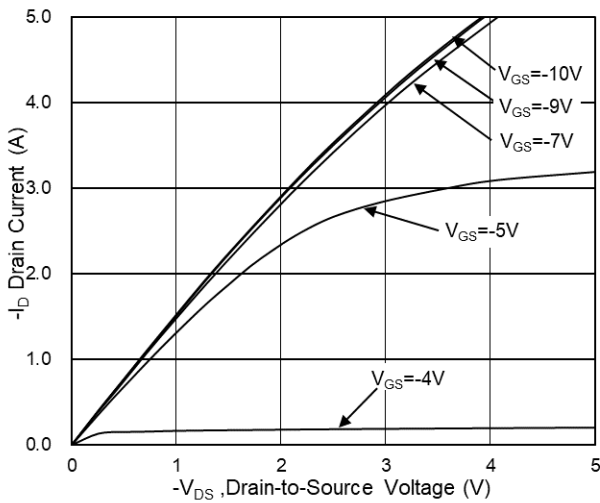


Fig.1 Typical Output Characteristics

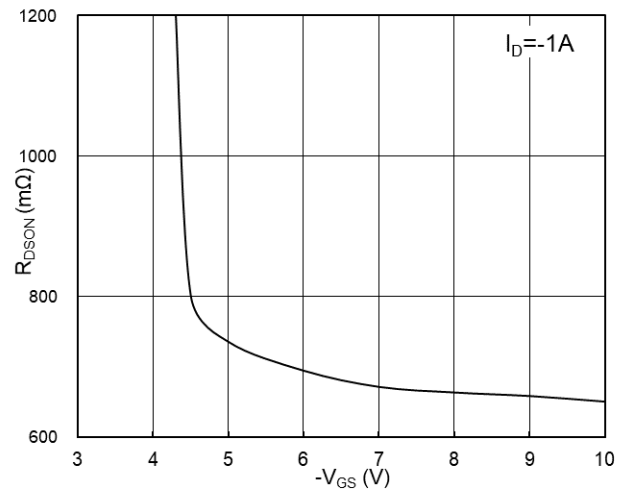


Fig.2 On-Resistance vs G-S Voltage

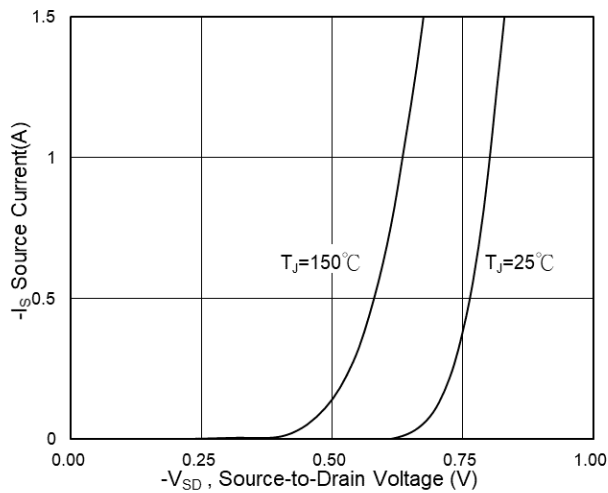


Fig.3 Source Drain Forward Characteristics

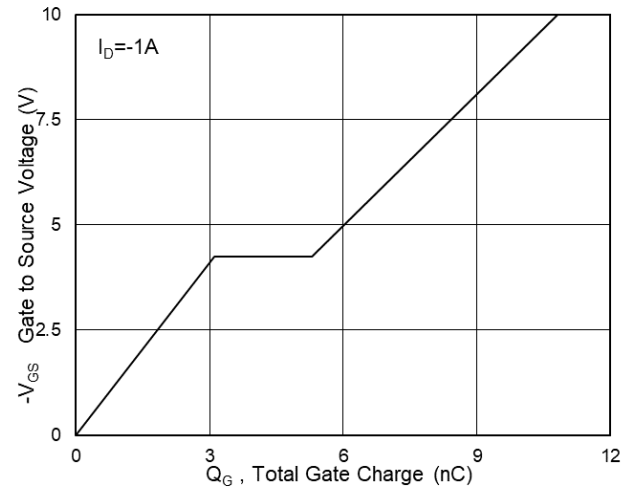


Fig.4 Gate-Charge Characteristics

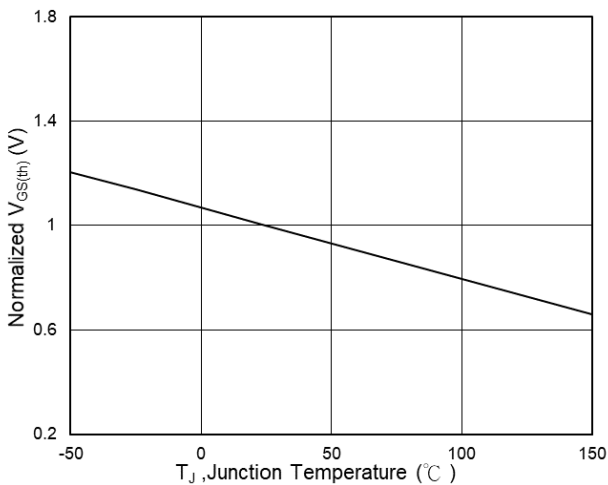


Fig.5 Normalized $V_{GS(th)}$ vs T_J

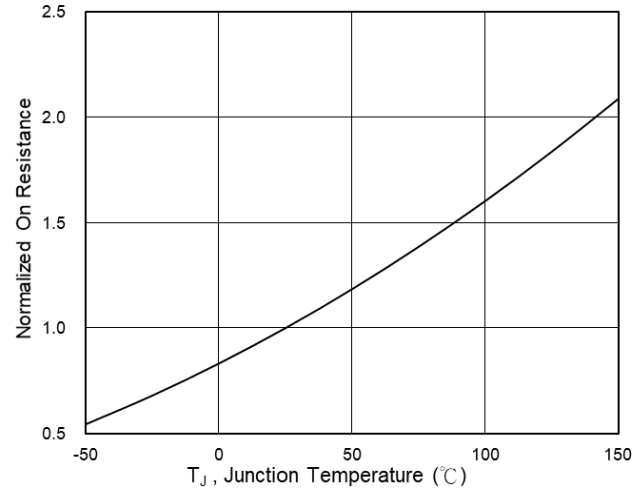


Fig.6 Normalized $R_{DS(on)}$ vs T_J



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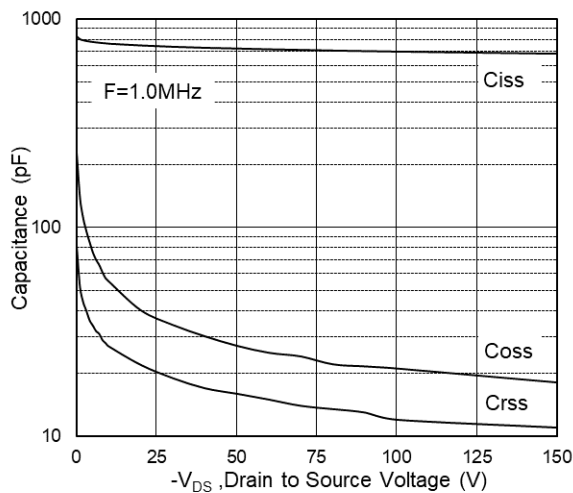


Fig.7 Capacitance

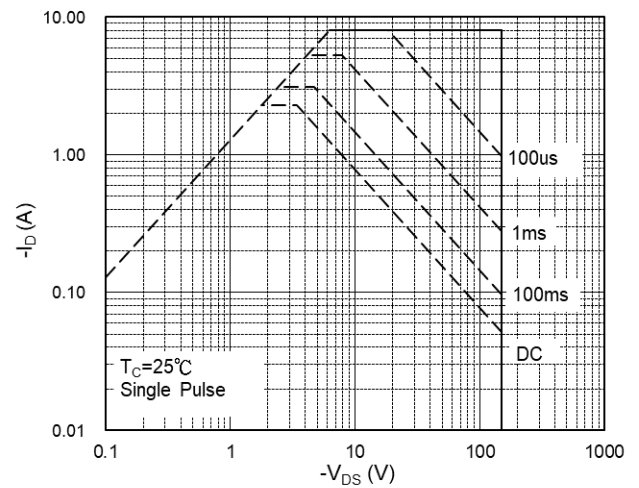


Fig.8 Safe Operating Area

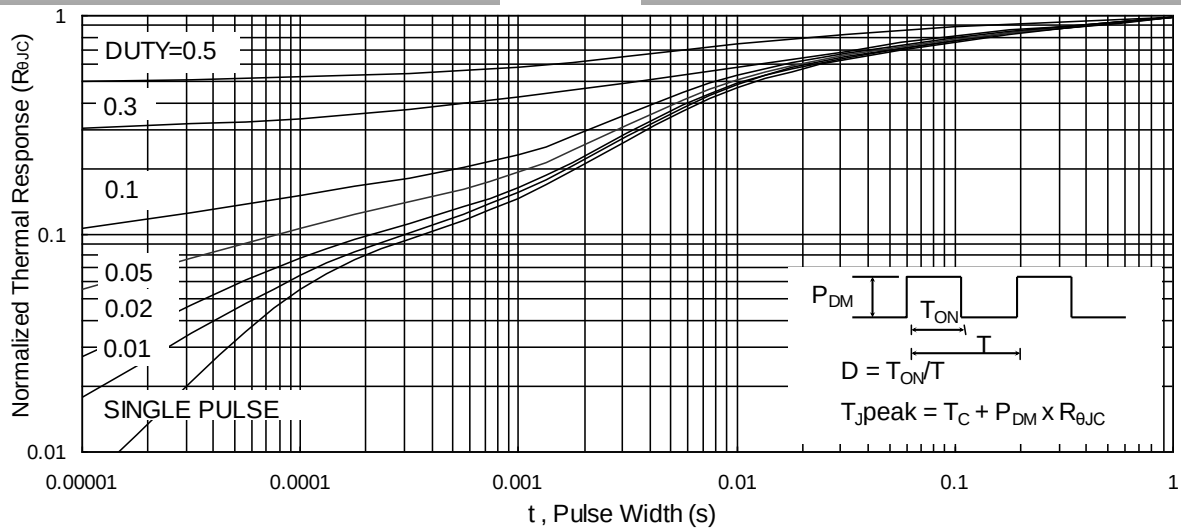


Fig.9 Normalized Maximum Transient Thermal Impedance

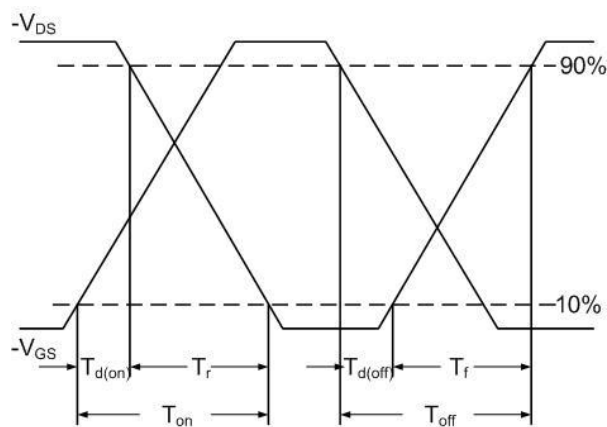


Fig.10 Switching Time Waveform

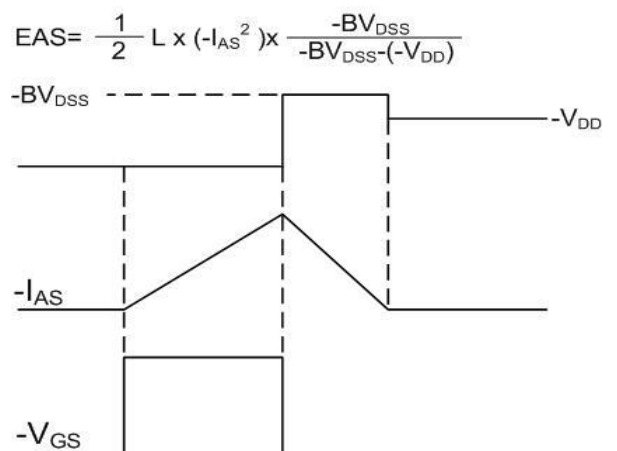
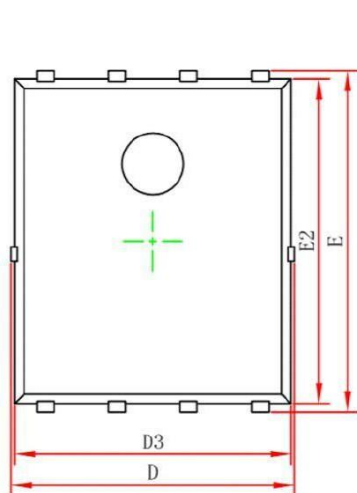
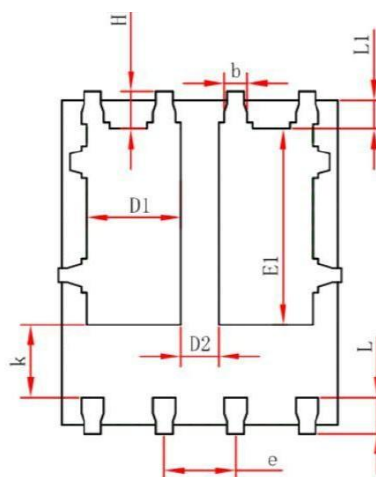


Fig.11 Unclamped Inductive Waveform

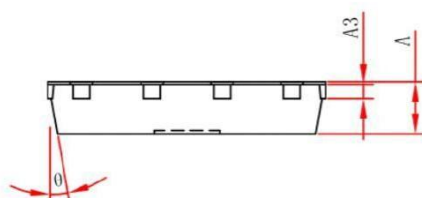
Package Mechanical Data- PDFN5060-8L



Top View



Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.154REF.		0.006REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	1.470	1.870	0.058	0.074
D2	0.470	0.870	0.019	0.034
E1	3.375	3.575	0.133	0.141
D3	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°