

P-Ch 20V Fast Switching MOSFETs

- ★ Super Low Gate Charge
- ★ Green Device Available
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

Product Summary



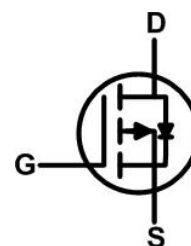
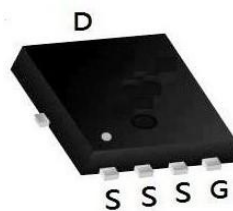
BVDSS	RDS(on)	ID
-20V	2.2mΩ	-120A

Description

The UD120P02F is the high cell density trench P-ch MOSFETs, which provide excellent RDS(on) and gate charge for most of the synchronous buck converter applications.

The UD120P02F meet the RoHS and Green Product requirement with full function reliability approved.

PDFN5060-8L Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-20	V
V_{GS}	Gate-Source Voltage	± 12	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	-120	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	-60	A
I_{DM}	Pulsed Drain Current ²	-480	A
EAS	Single Pulse Avalanche Energy ³	155	mJ
I_{AS}	Avalanche Current	25	A
$P_D@T_C=25^\circ C$	Total Power Dissipation ⁴	124	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	4.4	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	1.1	$^\circ C/W$

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Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-20	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =-1mA	---	---	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-4.5V, I _D =-30A	---	2.2	2.9	mΩ
		V _{GS} =-2.5V, I _D =-20A	---	3	4	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =-250uA	-0.55	-0.75	-1	V
$\Delta V_{GS(th)}$	V _{GS(th)} Temperature Coefficient		---	---	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-20V, V _{GS} =0V, T _J =25°C	---	---	-1	uA
		V _{DS} =-20V, V _{GS} =0V, T _J =100°C	---	---	---	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±12V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =-5V, I _D =-16A	---	---	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	5.1	---	Ω
Q _g	Total Gate Charge	V _{DS} =-10V, V _{GS} =0 to -10V, I _D =-30A	---	98	---	nC
Q _{gs}	Gate-Source Charge		---	20	---	
Q _{gd}	Gate-Drain Charge		---	25	---	
T _{d(on)}	Turn-On Delay Time	V _{GS} =-10V, V _{DS} =-10V, I _D =-30A, R _{GEN} =3Ω	---	19	---	ns
T _r	Rise Time		---	55	---	
T _{d(off)}	Turn-Off Delay Time		---	258	---	
T _f	Fall Time		---	138	---	
C _{iss}	Input Capacitance	V _{DS} =-10V, V _{GS} =0V, f=1MHz	---	10611	---	pF
C _{oss}	Output Capacitance		---	1368	---	
C _{rss}	Reverse Transfer Capacitance		---	901	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current ^{1,4}	V _G =V _D =0V, Force Current	---	---	-120	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =-11A, T _J =25°C	---	---	-1.2	V
t _{rr}	Reverse Recovery Time	I _F =-30A, di/dt=100A/μs	---	38	---	nS
Q _{rr}	Reverse Recovery Charge	μs, T _J =25°C	---	29	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- 2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3.The EAS data shows Max. rating . The test condition is T_J = 25°C, V_{DD}=-16V, V_{GS}=-4.5V, L=0.5mH.
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Performance Characteristics

Figure 5: Output Characteristics

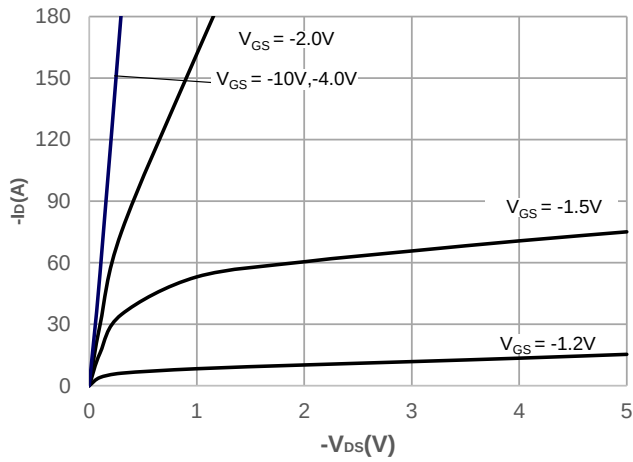


Figure 6: Typical Transfer Characteristics

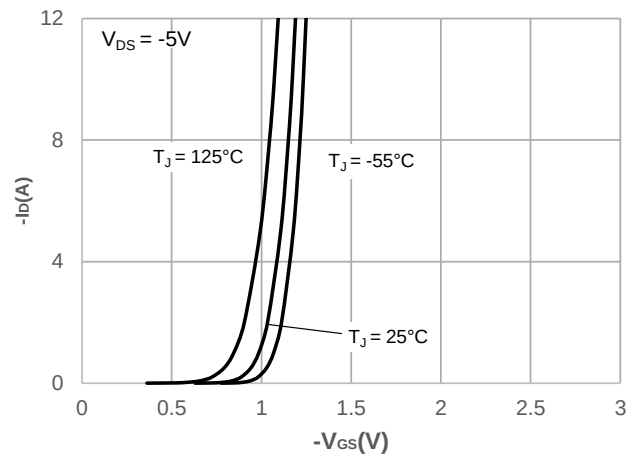


Figure 7: On-resistance vs. Drain Current

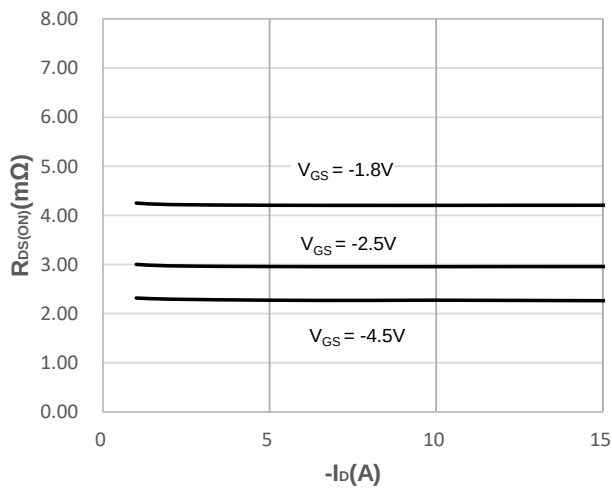


Figure 8: Body Diode Characteristics

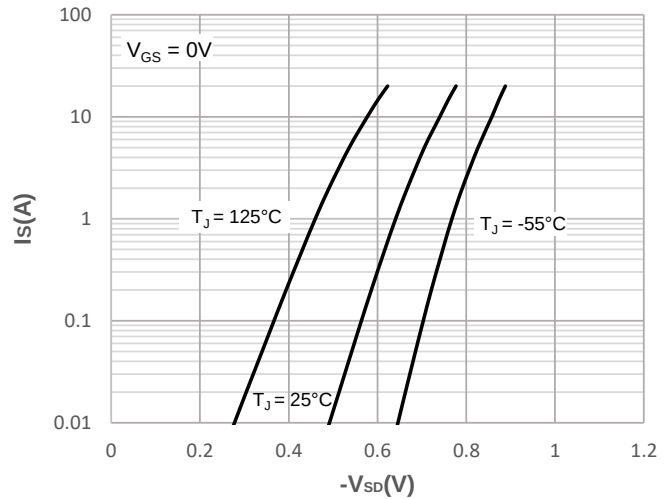


Figure 9: Gate Charge Characteristics

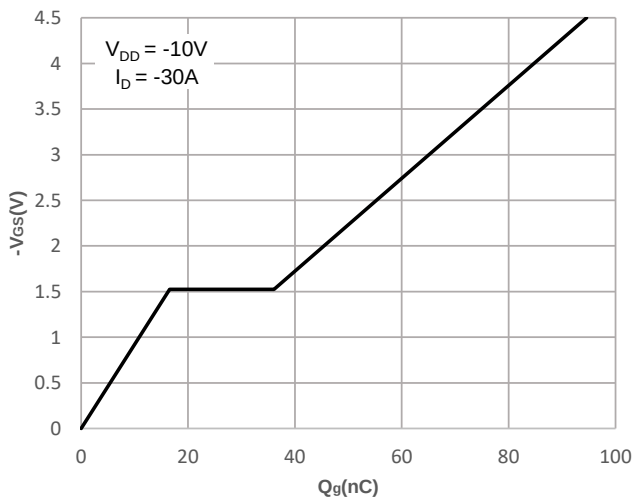
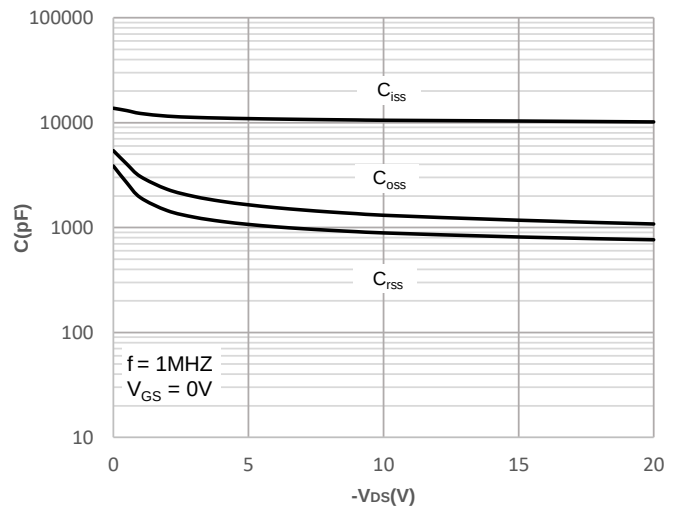


Figure 10: Capacitance Characteristics



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Figure 11: Normalized Breakdown voltage vs. Junction Temperature

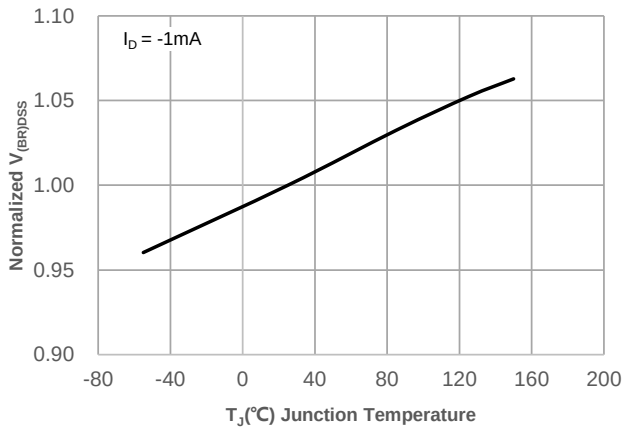


Figure 12: Normalized on Resistance vs. Junction Temperature

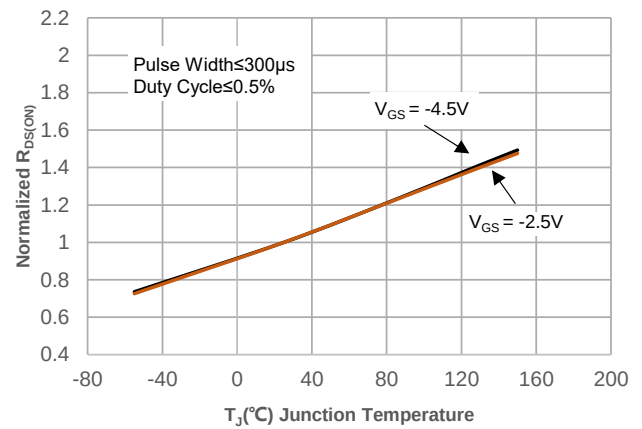


Figure 13: Normalized Threshold Voltage vs. Junction Temperature

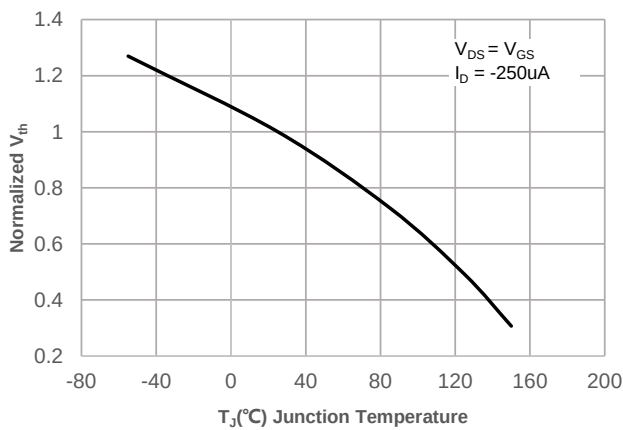


Figure 14: $R_{DS(ON)}$ vs. V_{GS}

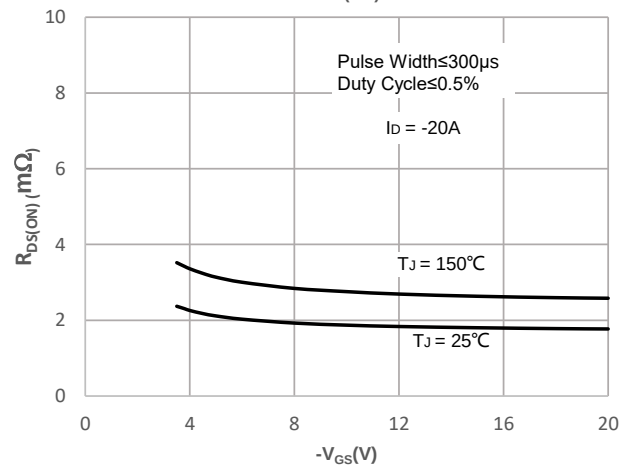
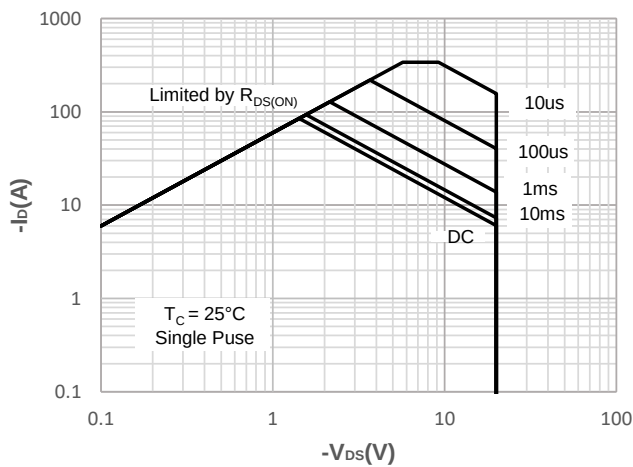


Figure 15: Maximum Safe Operating Area



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Figure 1: Power De-rating

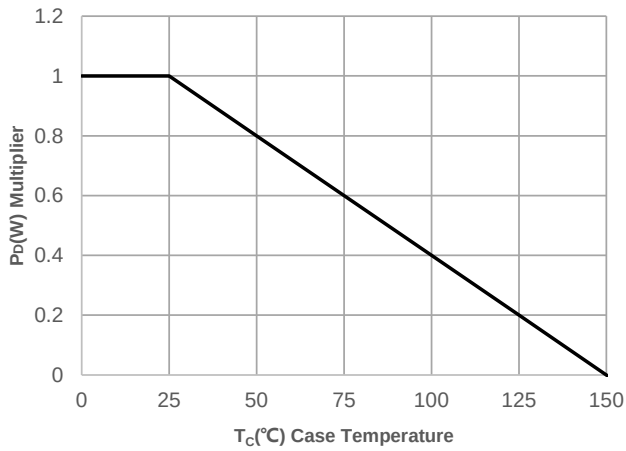


Figure 2: Current De-rating

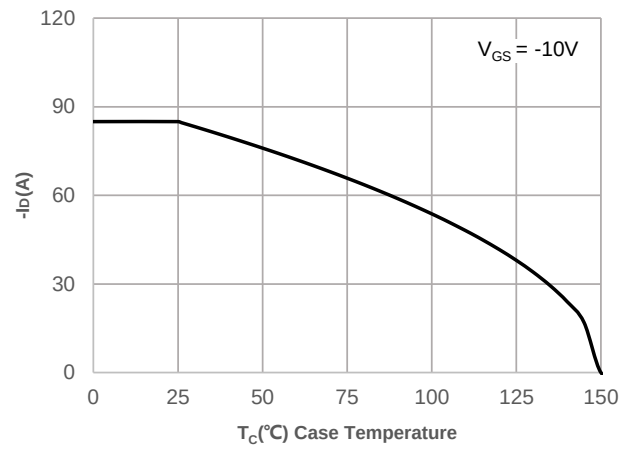


Figure 3: Normalized Maximum Transient Thermal Impedance

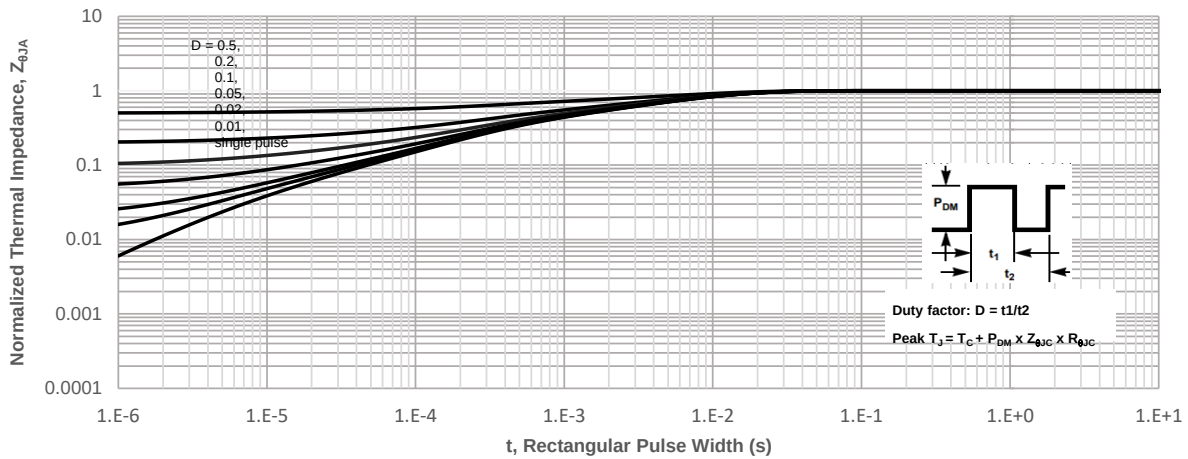
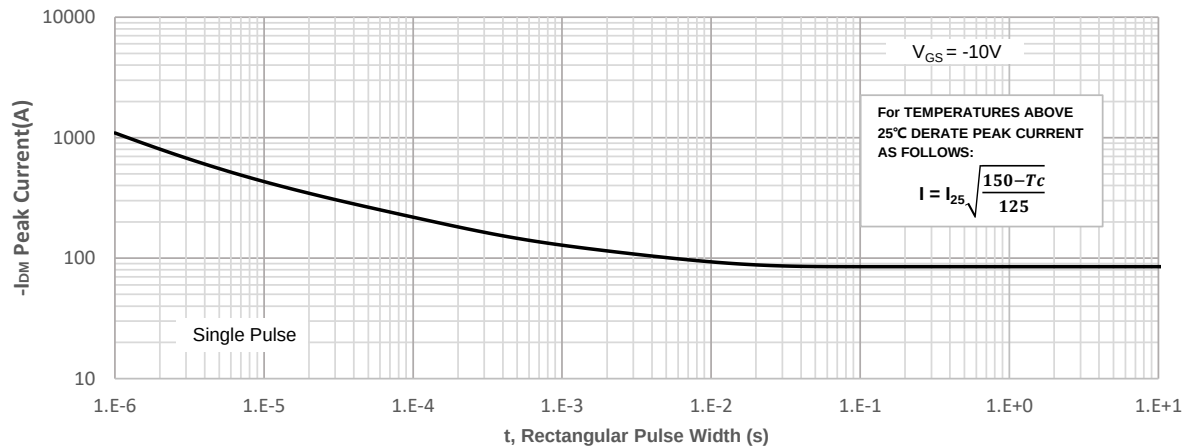


Figure 4: Peak Current Capacity



Test Circuit

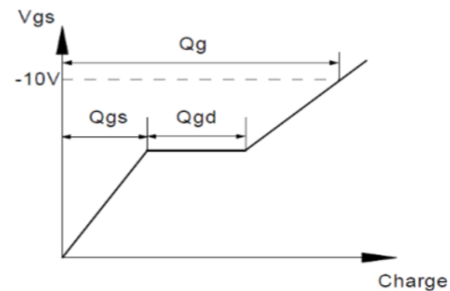
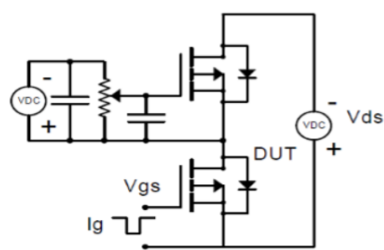


Figure 1: Gate Charge Test Circuit & Waveform

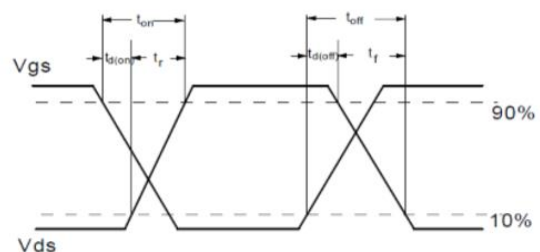
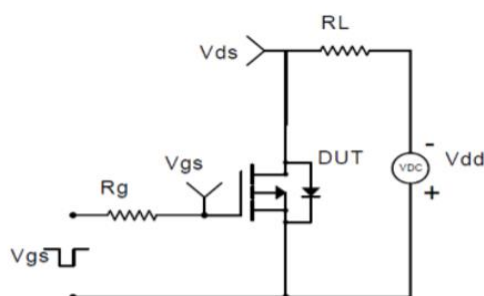


Figure 2: Resistive Switching Test Circuit & Waveform

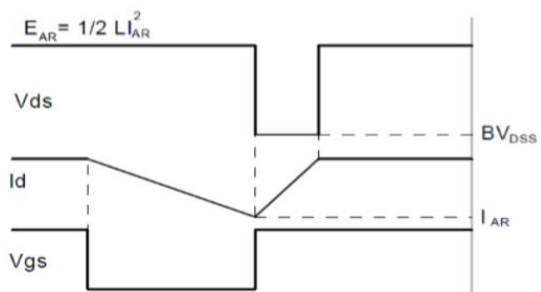
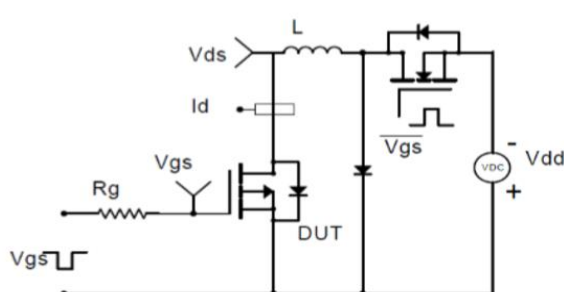


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

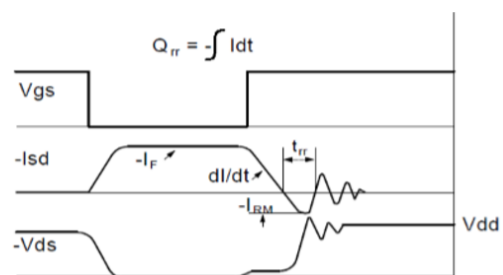
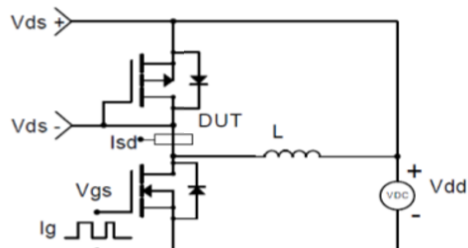
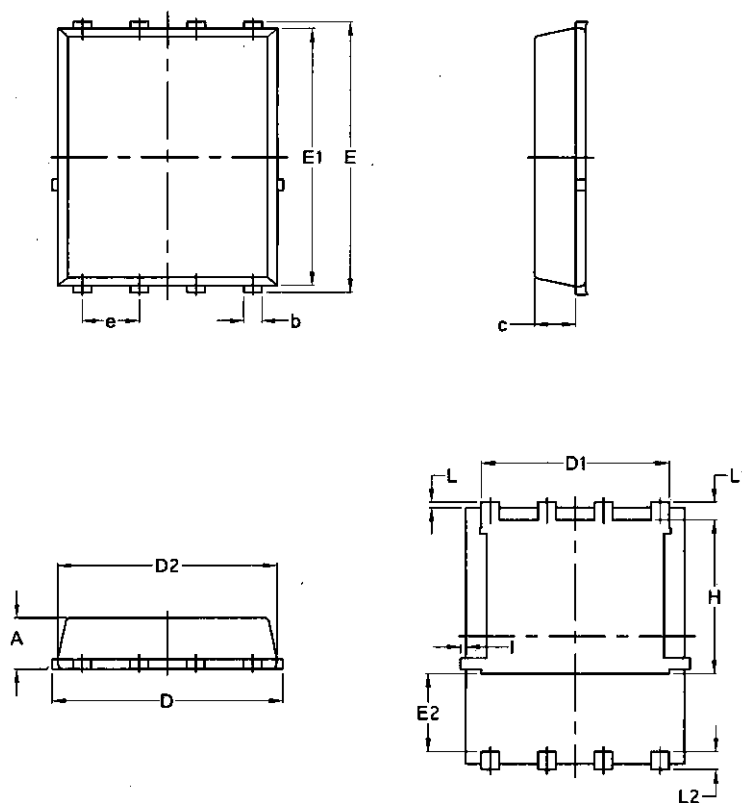


Figure 4: Diode Recovery Test Circuit & Waveform

Package Mechanical Data-PDFN5060-8L-Single



Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070